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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/758,520	01/15/2004	In-Hwan Oh	24317/82851	5805

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EXAMINER	
PHILOGENE, HAISSA	
ART UNIT	**PAPER NUMBER**
2828	

DATE MAILED: 11/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/758,520	OH, IN-HWAN	
	Examiner	Art Unit	
	Haissa Philogene	2828	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16 and 21-28* is/are rejected.

7)☒ Claim(s) *17-20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *01/15/04;06/23/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3, 4, 6, 7, 9, 12, 13, 15, 16, and 23-28 are rejected under 35 U.S.C. 102(b) as being anticipated by Wang et al, Patent No. 6,337,544.

As per claim 1, Wang discloses in Fig.1 a lamp-control circuit, comprising a power factor corrector (12); a digitally controlled ballast (10, 11), comprising power devices (T1, T2 or 7) and coupled to the power factor corrector (12), the ballast operable to power a lamp (R_L); a current feedback loop (R, 4), coupled between at least one of the power devices (T2) and the digitally controlled ballast (10, 11); and a voltage feedback loop (VI, 3), coupled between the lamp (R_L) and the digitally controlled ballast (10, 11).

As per claim 3, Wang discloses the digitally controlled ballast (10, 11) comprising: a controller (10), coupled to the power factor corrector (12) by a DC link (as shown); and an output stage comprising the power devices (T1, T2, or 7) and coupled to the controller (10).

As per claim 4, Wang discloses the controller (11) comprising: a digital controller (20), coupled to the power factor corrector (12) by the DC link; and a power device driver (8), controlled by the digital controller (20) via PWM (31) and configured to drive the output stage (T1, T2, or 7).

As per claim 6, Wang discloses the output stage comprising two MOSFET power devices (T1, T2, or 7) coupled in series having an output terminal via a node (as shown) coupled in between the MOSFET power devices.

As per claim 7, Wang discloses the current feedback loop (4) comprising a current sensor R (not labeled), coupled to the two power devices (T1, T2), thereby operable to sense the current of at least one power device (T2).

As per claim 9, Wang discloses the voltage feedback loop (3) comprises a voltage sensor via DLSP (20), coupled to the lamp (R_L), thereby operable to sense the voltage of the lamp (see abstract, lines 1-2).

As per claims 12 and 13, Wang discloses in Fig.1 the digitally controlled ballast (10) being configured to receive external commands (COM) while in operation, and the lamp-control circuit (Fig.1) being operable to power a lamp (R_L) being a fluorescent lamp (see Col.1, line 5).

As per claims 15 and 16, Wang discloses a method of operating a lamp-control circuit (see Fig.1), the circuit comprising a digital controller (10), an output stage (T1, T2, C1, L1, C2, Cp, TE, R_L), a current feedback loop (2 or 4), and a voltage feedback loop (3), the method comprising: receiving one of a current feedback signal and a voltage feedback signal by the digital controller (10) through DLSP (20); generating a digital control signal (6) from DLSP (20) and PWM (31) in response to the received signal by the digital controller (10) through DLSP (20) ; and powering a lamp R_L by the output stage according to the generated digital control signal (6); wherein the generating of a

digital control signal (6) comprising the step of generating a pulse width modulated control signal (6) by the digital controller (10) through PWM (31).

As per claim 23, Wang discloses the steps or sensing a current of the output stage by the current feedback loop (4 or 2) which includes a sensed resistor R (as shown); generating the current feedback signal (4 or 2) according to the sensed current, receiving the current feedback signal (4 or 2) by the digital controller (10) through DLSP (20); and controlling the frequency of the digital control signal (6) by DLSP (20) and PWM (31) to control the received sensed current into a predetermined range.

As per claim 24, Wang discloses the steps or sensing a voltage of the lamp (Vl) by the voltage feedback loop (3); generating the voltage feedback signal (3) according to the sensed voltage; coupling the voltage feedback signal (3) into the digital controller (10) through ADC (23) and DLSP (20); and controlling the frequency of the digital control signal (6) by DLSP (20) and PWM (31) to control the received sensed voltage into a predetermined range.

As per claim 25, Wang discloses the step of generating the digital control signal (6) to control at least a lamp preheating time set by MCU (14) (see Col.3, lines 7-14).

As per claim 26, Wang discloses the step of generating the digital control signal (6) to provide at least an over-load protection or over-current protection by extracting peak values of lamp current (2) and lamp voltage (3) through digital substract (21) of DLSP (20) (see Col.3, lines 24-26 and see Col.1, lines 62-65).

As per claim 27, Wang discloses the steps of receiving external control commands COM by the digital controller (10) during the operation of the lamp control circuit (Fig.1);

and sending status signals (6) by the digital controller (10) upon calculation of the input digital lamp current and voltage signals via DSLP (20) during the operation of the lamp control circuit.

As per claim 28, Wang discloses the receiving the external control commands comprises: receiving external commands COM via CPCM by the digital controller (10) to vary a frequency of the digital control signal (6) via PWM (31) to digitally control the operation of the lamp by regulating the lamp power or lamp current at a selected level , i.e., the brightness of the lamp.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang in view of Ribarich, Patent No. 6,956,336.

As per claim 2, Wang discloses the claimed invention substantially as explained above. Wang does not explicitly disclose the PFC being operable to generate AC input

current and voltage essentially in phase with each other. Ribarich discloses in Fig.2 a lamp-control circuit having a PFC via M3 being operable to generate AC input current and voltage essentially in phase with each other (see Col.2, lines 65-67). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to employ the PFC as taught by Ribarich into the Wang type circuit, because it would allow a sinusoidal line input current in phase with the input voltage for high power factor as seen from the input power source, thereby maintaining total harmonic distortion at low levels.

As per claim 5, Wang discloses the claimed invention substantially as explained above. Further, Wang discloses the digital controller (20) and the power device driver (8) each being in a separate chip and also integrated single chip design (see abstract. Wang does not disclose the digital controller and the power device driver being integrated on a chip. Ribarich discloses in Fig.2 a lamp-control circuit having a controller and a power device driver being integrated on a chip (U1). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to employ the IC chip as taught by Ribarich into the Wang type circuit, because it would allow a reduction in manufacturing and design costs while providing a robust operation in the system.

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al in view of Jales et al., Patent No. 6,879,114.

Wang discloses the claimed invention substantially as explained above. Further, Wang discloses the current sensor R (not labeled) being a current sensing resistor,

coupled in series with the two power devices (T1, T2). Wang does not disclose the current feedback loop comprising a resistor-capacitor filter, coupled between the current sensing resistor and the digital controller. Jales discloses in Figs.1 and 2 a lamp-control circuit having a current feedback loop comprising a resistor-capacitor filter (R19, C10 or LPF), coupled between a current sensing resistor (R18 or Rsense) and a controller (CTRL) via current control amplifier (CC). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to employ the resistor-capacitor filter as taught by Jales into the Wang type circuit, because it would allow an accurate control of the lamp brightness upon measurement of the current flowing into the circuit.

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wang in view of Gradzki et al., Patent No. 6,011,360.

Wang discloses the claimed invention substantially as explained above. Wang does not disclose the voltage sensor being a voltage sensing resistor, coupled to the lamp; and the voltage feedback loop comprising a resistor-capacitor filter, coupled between the voltage sensing resistor and the digital controller. Gradzki discloses in Fig.1 a lamp-control circuit having a voltage sensor being a voltage sensing resistor (930) (see also Col.7, lines 36-40), coupled to a lamp (85); and a voltage feedback loop comprising a resistor-capacitor filter (930, 189, 183) (see also Col.6, lines 7-10), coupled between the voltage sensing resistor (930) and a controller (109). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to employ the voltage sensing resistor and the resistor-capacitor filter as taught

by Gradzki into the Wang type circuit, because it would allow a control of the lamp brightness upon receiving an average value of the lamp voltage.

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wang in view of Mader et al., Patent No. 6,469,454.

Wang discloses the claimed invention substantially as explained above. Wang does not disclose the digital controller comprising a comparator, configured to compare a signal of at least one of the current feedback loop and the voltage feedback loop to a reference voltage. Mader discloses in Fig.1 a lamp-control circuit having a digital controller (dotted box) comprising a comparator (68), configured to compare a signal of a current feedback loop via pin CS to a reference voltage (0.45V). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to employ the comparator as taught by Mader into the Wang type circuit, because it would allow a voltage control to keep the buck converter in an off state.

Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wang in view of Ribarich, Patent No. 6,008,593.

Wang discloses the claimed invention substantially as explained above. Wang does not disclose the lamp-control circuit being operable to control more than one lamps, wherein the lamps are coupled to corresponding voltage feedback loops. Ribarich discloses in Fig.6A a lamp-control circuit being operable to control more than one lamps (24), wherein the lamps (24) are coupled to corresponding voltage feedback loops via pins CS1 and CS2 (see Col.7, lines 7-8). It would have been obvious to a person having ordinary skill in the art at the time the invention to employ the lamps as taught by

Ribarich into the Wang type circuit, because it would allow one lamp to continue to operate even when the other lamp is removed or a filament is open.

Claims 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang in view of Ribarich, Patent No. 6,150,773.

As per claim 21, Wang discloses the claimed invention substantially as explained above. Wang further discloses lamp preheating and ignition (Col.3, lines 9-10). Wang does not explicitly disclose powering the lamp comprising: pre-heating the lamp by powering the lamp at a pre-heating frequency, wherein at the pre-heating frequency the voltage across the lamp is below an ignition voltage. Ribarich discloses in Fig.16 a lamp-control circuit having a step of powering a lamp (as shown) which comprises pre-heating the lamp by powering the lamp at a pre-heating frequency (43.9 KHz), wherein at the pre-heating frequency the voltage across the lamp (307.4V) is below an ignition voltage (650V) (see Fig.18). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to employ lamp preheating as taught by Ribarich into the Wang type circuit, because it would allow optimization of the lamp ballast size and cost, thereby reducing ballast product families and increasing manufacturability.

As per claim 22, Wang in view of Ribarich discloses the claimed invention substantially as explained above. In addition, Ribarich discloses powering the lamp comprises: igniting the pre-heated lamp (as shown) by powering the lamp at a lower ignition frequency (38.3 KHz), wherein at the ignition frequency the voltage across the lamp

(high voltage) inherently exceeds an ignition voltage since the voltage increases as the frequency decreases.

Allowable Subject Matter

Claims 17-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: The prior art fails to disclose the following recited limitations: "wherein generating a pulse frequency modulated signal comprises: generating a counter signal by increasing a voltage level in accordance with increasing counter values; and generating a control voltage" (claim 17); or "wherein generating a pulse width modulated control signal comprises: generating a counter signal by increasing a voltage level in accordance with increasing counter values; and generating a control voltage, varying in time" (claim 20).

Correspondence

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Haissa Philogene whose telephone number is (571) 272-1827. The examiner can normally be reached on 8:30 A.M.-6:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, MinSun Harvey can be reached on (571)272-1835. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

hp

Haissa Philogene
Primary Examiner